Mercury TCD Electronics Circuit Description
Revision: 1
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1. Applicability

This document applies to Mercury TCD schematic 03-925040-00, Revision PR3.

2. Power supplies and grounds

There are four grounds serving the TCD electronics circuitry. Ground 1 is the return for the +5V digital supply. It is connected directly to Ground 4, the unregulated +24V return, at the card edge connector on the Mother board. The analog return is Ground 2, which provides a low-noise return for the ±15V and +5.25V supplies. Ground 3 is the reference for analog signal distribution, which carries almost no DC current. All of the grounds must be tied together externally for the board to function properly.

Three RC filters remove noise from the analog power supplies. These consist of R39 with C28, R40 with C29, and R41 with C30.

3. Digital circuits

U8 decodes bus address information to access latch U6, buffer U9, and DACs U3 and U4. The latch holds all of the digital control signals for the board, while the buffer transmits the board identification number and filament temperature limit status to the bus. R42 allows the inputs of U9 to be pulled high for test, while remaining low in normal operation.

4. Power Converter

The TCD requires a variable, stable, floating excitation source, which is derived from the unregulated +24V instrument supply. U1 is a current-mode switching regulator controller, operating as a flyback regulator at 40kHz. Its internal pass transistor is connected between pin 4 (VSW) and pin 3 (ground). When the switch turns on, the primary current of T1 begins to increase at about 0.8A/μs. Current flow stops abruptly when the switch turns off, causing the voltage at U1-4 to rise rapidly. CR8 and VR3 clamp the voltage at 25V above the input supply voltage, conducting until the energy stored in the leakage inductance of T1 is gone. VR2 does not normally conduct, but will protect U1 if a transient raises the +24V supply excessively.

When the primary current is interrupted, and the voltage on primary pin 5 of the transformer rises, the voltages on secondary pins 7 and 10 also go positive. Diodes CR2 and CR9 are then forward biased, allowing current to flow in both secondaries. Because the secondaries are bifilar wound, the voltages across the secondary windings remain

equal to each other throughout the cycle. The main output from CR9 is smoothed by C7, and the high-frequency ripple and noise are further attenuated by L1, L2, C3, and C5. The rectified voltage across C4 is equal to the main output voltage, which is floating. This provides a ground-referenced feedback signal, allowing the output voltage to be controlled without any direct connection to the main secondary circuit. Leakage inductance in T1 degrades the tracking accuracy between the two secondary voltages. This effect is reduced by loading the sense output with R2, and by choosing CR2 to have a longer recovery time than CR9.

The sense voltage at C4 is combined through R4, R5, and R26 with the output of the bridge voltage control DAC at AR4-1, which varies between 0 and -10V. U1 adjusts its conduction duty cycle to try to hold its feedback pin (pin 2) at 1.24V. The output voltage across C7 follows the DAC setting according to the following equation:

$$V_{out} = -3.14 * V_{DAC} + 4.14.$$

CR3 prevents the output voltage from falling below about 10V at low DAC settings, so that the circuitry powered by the floating supply remains active. CR4 keeps U1-2 from going negative if the DAC is set to a large (negative) output while the converter is disabled, which would otherwise cause U1 to lock up. High-frequency noise between ground 4 and ground 2 is filtered off of the control signal by C11, to avoid instability in the switching converter. C1 and R3 provide feedback loop compensation for U1, and CR5 holds the control pin of U1 (pin 1) low when U6-19 is low, thus turning off the converter.

5. Bridge voltage regulator and monitor

The TCD bridge excitation voltage is set by the bridge voltage control DAC, U3. AR1 converts the current output from the DAC to a voltage, which varies from 0 to -10V at the amplifier output. C16 reduces digital noise interference. The DAC output is shifted and attenuated by R18 (pins 3, 4, 13, and 14) to create a control voltage that remains within the common mode range of buffer AR2, which is powered from the floating power supply. The high impedance input of AR2 virtually eliminates any current from the ground-referenced DAC circuitry from flowing into the floating circuitry, which would cause a signal offset as the current flowed back to ground through the bridge. Two more sections of R18 divide the 10-volt reference by two, and the other section of AR2 buffers the connection to the floating circuit. A differential control voltage, which varies from 0 to -5V between AR2-7 and AR2-1, is thus available to set the bridge excitation voltage.

The remaining sections of R18, combined with R19, R20, and AR3, form a differential amplifier with a gain of 5.62, referenced to the return side of the floating supply. The feedback is taken from the supply side of the TCD bridge, so the amplifier output tries to force the bridge voltage to be 5.62 times the differential control voltage between R18-5 and R18-6. The feedback path is completed from AR3-1 through CR11, VR1, and R6, to the supply side of the bridge. Regulator VR1 has internal circuitry which holds its output

(pin 2) 1.25 volts above its adjust pin (pin1). It also supplies current limiting and thermal overload protection, in the event of excessive load. C6 provides a low impedance at the input of VR1 at high frequencies, to maintain stability of the regulator. C12 stabilizes the overall loop response.

Excitation voltages, bridge current, and signal voltage are all available for measurement at the card edge connector. Analog switch U5 connects one of these four voltages at a time to P1-3, depending upon which output of decoder U8 is low. The selection is made by latching the appropriate value into U6, pins 12 and 15. The bridge supply and return voltages are divided by 50.9 through resistors R33, R34, R35 and R36. The bridge signal voltage is divided by 11 through R38 and R37, in order to minimize the disturbance to the signal amplifier when a direct measurement is made through switch U5. Bridge current is sensed by measuring the voltage drop across R6 with differential amplifier AR4 (pins 5-7). The amplifier gain is 1, so the scale factor of the voltage at P1-3 is 200mA/V.

6. Temperature limit circuit

In normal operation, the filaments of the thermal conductivity detector bridge rise and fall in temperature as the surrounding gas composition changes. Since the filaments have a positive temperature coefficient of resistance, their peak temperature can be limited by reducing the bridge excitation voltage whenever a filament reaches a preset maximum resistance. Resistors R9, R10, and R6 form a bridge circuit with the bridge element connected between J1-5 and J1-3. With K1 closed, the inputs of amplifier AR1 (pins 2 and 3) are connected across this bridge. When the filament resistance reaches about 82Ω, the temperature-sensing bridge is balanced, and the output of AR1 (pin 1) begins to drop. This pulls down the adjust pin of VR1 through CR6 and U2, decreasing the detector excitation, and holding the filament resistance at the preset limit.

The other half of AR1 amplifies the output of a similar bridge, which senses the resistance of the filament connected between J1-5 and J1-2, using resistors R6, R13, and R14. The outputs of both halves of AR1 are combined with the output of the main control amplifier, AR3, through diodes CR11, CR6, and CR7. Whichever amplifier calls for the lowest bridge excitation controls the loop, with the other amplifier outputs both at the positive supply rail. C2 stabilizes the loop when one of the temperature-limit amplifiers is in control. Opening K1 effectively raises the point on R6 where the inverting inputs of AR1 are connected, thereby lowering the filament resistance which is required to cause limiting.

As long as AR3 is in control of the loop, the 1.25V differential between pins 1 and 2 of VR1 appears across the base-emitter junction of Q2 and R7. Q2 sources about 6mA into optocoupler U2, turning it on, and bringing its output (pin 7) low. When temperature limiting occurs, sending the output of AR3 to the positive rail, CR10 becomes reverse biased. This turns off Q2 and U2, and indicates the limit condition with a high level on the output of U2.

To maintain normal bridge voltage control with no detector plugged in, the temperature-limit circuit must be defeated. U2 disconnects the outputs of the limit amplifiers from VR1 when it is turned off, by setting a logic high at U6 pin 2.

7. Bridge balance DAC and signal amplifier

Bridge signals down to one microvolt must be detected by the instrument, so it is necessary to have the bridge balanced to within 1mV or less for efficient digitization of the signal. Balance is adjusted by DAC U4 and the associated circuitry. Four sections of R21, a precision-tracking network, provide an effective shunt resistance of 1K across the bridge element connected between J1-3 and J1-4. The reference voltage to the DAC is just exactly the voltage across this resistance. The DAC inverts this voltage, and multiplies it by the ratio of the DAC setting to 4096. The DAC output voltage is applied to a 500Ω resistance, consisting of two paralleled sections of R21, which sources current into the bridge at J1-3 (which is also Ground 3). Since this current can be as high as 28mA, Q3 is used to boost the current output capability of amplifier AR5 (pin 1). When the DAC is set to mid-scale, the variable current through the 500Ω resistance exactly cancels the current through the fixed 1K shunt, and there is no effect on the bridge balance. Setting the DAC either above or below 2048 allows the bridge to be offset in either direction.

For the DAC to work properly, pin 2 (AGND) must be held at the same voltage as pin 1 (IOUT), which is at Ground 3. However, the current from this pin must be returned directly to the floating supply, so the current does not have to flow back through the bridge. AR5 (pins 5-7) buffers Ground 3 for this purpose. C17 and C21 reduce the effect of digital noise on the balance circuit.

The bridge signal at J1-2 is amplified by AR6. Gain is set to 2, 20, or 200, by closing one of the switches of U7. Only one switch should be closed at a time. C23 sets the time constant of the amplifier to 50ms for noise reduction. The capacitors connected to the inputs of AR6 all reduce digital noise interference, and R30 and C27 also attenuate noise from the switching power converter noise. R28 and C31 reduce the disturbance caused by switching the loads connected to the output of AR6.

Signals from the bridge balance circuit appear at the signal amplifier only if a bridge is connected. In order to be able to test the circuit board without a detector, a high-resistance bridge (R17) is always present on the board, in parallel with the normal detector connection. All of the board functions are operational in this state, but the balance control is about 40 times more sensitive, due to the greater bridge resistance. As noted in the preceding section, the temperature limit function must be defeated for the circuit to operate without an external bridge.

8. Log of revisions and file identification

Rev. 1 4/10/95

File: engrserv:\3800elec\doc\TCDCD.DOC

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